CLAIMS:

1. An electrical switch circuit comprising:

a first, second, and third ceramic substrate positioned in juxtaposed relationship with each other;

a first electrical device coupled to the first and second substrates and positioned there between; and

a second electrical device coupled to the second and third substrates and positioned there between, the second electrical device being electrically coupled to the first electrical device.

2. The electrical switch circuit of claim 1, further including a first, second, and third terminal, the first terminal coupled to the first substrate and electrically coupled to the first electrical device, the second terminal coupled to the first and second substrates and electrically coupled to the first and second electrical devices, the third terminal coupled to the second and third substrates and electrically coupled to the second electrical device.

3. The electrical switch circuit of claim 2, wherein the first, second, and third terminals have a rectangular cross-section.

4. The electrical switch circuit of claim 2, wherein the first and third terminals are positioned substantially in registry with each other.

5. The electrical switch circuit of claim 1, further including a first and second resistor, the first resistor coupled to the first substrate and electrically coupled to the first electrical device, the second resistor coupled to the second substrate and electrically coupled to the second electrical device.

6. The electrical switch circuit of claim 1, wherein the first and second electrical devices include transistors.

7. The electrical switch circuit of claim 6, wherein the transistors include insulated gate bipolar transistors.

8. The electrical switch circuit of claim 6, wherein the transistors include metal oxide semiconductor field-effect transistors.

9. The electrical switch circuit of claim 6, further including a first and a second gate pin, the first gate pin coupled to the first and second substrates and electrically coupled to the first transistor, the second gate pin coupled to the second and third substrates and electrically coupled to the second transistor.

10. The electrical switch circuit of claim 6, wherein the first and the second transistors are electrically coupled in a half-bridge electrical configuration.

11. The electrical switch circuit of claim 1, wherein the first device includes a diode.

12. The electrical switch circuit of claim 1, wherein the second device includes a diode.

13. The electrical switch circuit of claim 1, wherein the first and the second substrates include a plurality of vias.

14. The electrical switch circuit of claim 13, further including a conductive material positioned in the vias of the first and second substrates.

15. The electrical switch circuit of claim 1, wherein the first, second, and third substrates include an electrically conductive film formed on a surface of the first, second, and third substrates, the electrically conductive metal film facilitating electrical coupling between the first and second electrical devices.

16. The electrical switch circuit of claim 15, wherein the electrically conductive film is an electrically conductive thick film ink.

17. The electrical switch circuit of claim 15, wherein the electrically conductive film is a copper film.

18. The electrical switch circuit of claim 15, wherein the electrically conductive film is an aluminum film.

19. The electrical switch circuit of claim 15, wherein the electrically conductive film is an electrically conductive epoxy.

20. The electrical switch circuit of claim 15, wherein the electrically conductive film is formed using any of an evaporation process, a printing process, a sputtering process, and a brazing process.

21. The electrical switch circuit of claim 15, wherein the top planar geometry of the electrically conductive film is a substantial mirror image of the top planar geometry of a top surface of the first and second electrical devices.

22. A three phase inverter comprising:

a first, second, and third ceramic substrate positioned in juxtaposed relationship relative to each other;

a first and second transistor, the first transistor being coupled to the first and second substrates and positioned there between, the second transistor being coupled to the second and third substrates and positioned there between, the first and second transistors being electrically coupled together in a half-bridge electrical configuration;

a third and fourth transistor, the third transistor being coupled to the first and second substrates and positioned there between, the fourth transistor being coupled to the second and third substrates and positioned there between, the third and fourth transistors being electrically coupled together in a half-bridge electrical configuration; and

a fifth and sixth transistor, the fifth transistor being coupled to the first and second substrates and positioned there between, the sixth transistor being coupled to the second and third substrates and positioned there between, the fifth and sixth transistors being electrically coupled together in a half-bridge electrical configuration.